On-Chip Thermal Management Technique for Low-power CMOS circuits

Mr.P.Thirumurugan,
Assistant Professor, Department of ECE,
PSNA College of Engineering and Technology,
Dindigul, Tamil Nadu, India

Dr.S.Sasikumar,
Professor & Head, Department of ECE,
Jayaram College of Engineering and Technology,
Trichy, Tamil Nadu, India

***Abstract*—Power Consumption is a major bottleneck of system performance and is listed asone of the top three challenges in ITRS 2008.Leakage power dissipation becomes dominant in total power as technology scales. As reliability is concerned Negative Bias Temperature Instability (NBTI) becomes an important problem for circuit designers. There has been a large amount of work on leakage power and NBTI power degradation. Standby techniques focus mainly on reducing leakage and NBTI degradation that are in idle state, whereas runtime techniques focuses on reducing these effects in active devices. Most of the prior works focuses on reducing NBTI induced degradation and standby leakage power by considering their input dependency, but they are effective for smaller circuits only. We propose a mechanism which has an on-chip cooling mechanism called as dynamic thermal management (DTM) technique with already existing gate replacement techniques, which is used by high performance processor chips or date centers of which power consumption densities are high. The power dissipates as heat which will cause the increase of device temperatures. DTM controls the temperature actively by managing the power dissipation and/or cooling mechanisms and minimized the performance penalty. Compared with power management which aims at reducing total power energy consumptions DTM is dedicated to control the run – time on-chip temperature. Experimental results on bench marks show that the proposed technique can improve the gate replacement leakage optimization by 8-10%.** *(Abstract)*

Keywords- dynamic thermal management (DTM), gate replacement, low power, leakage power, negative bias temperature instability (NBTI)

I. INTRODUCTION

To overcome NBIT, the precious works however estimated the NBTI induced lifetime degradation with the assumptions that the circuits operate all the time.

The DTM is designed for reducing both spatial & temporal power consumption. In large circuits we cannot use Input vector control (IVC) technique, the gate replacement techniques such as Divide and conquer-based gate. replacement (DCBGR) can be combined with this proposed DTM technique to reduce the leakage power in large circuits by reducing both bias temperature and on-chip temperature. The need for controlling on-chip temperatures are listed below, they are

Increasing Reliability – The Temperature increase and high temperature gradients will cause negative temperature instability which is a biggest threat to reliability of a semiconductor device. It also increase the concentration unbalance that leads to the increase in electromigration.Hence, when designing semiconductor device we have to take care of the above problem for providing better reliability High temperature will enhance Negative Bias Temperature Instability (NBTI) which is thermally activated. Not only high temperature if self, high temperature gradient is also a threat to reliability.

Improve the Performance – The operating temperature will influence the performance of a semiconductor device by affecting the parameters such as the threshold voltage, saturation velocity, etc, this introduces mobility degradation which causes worse timing performance. Due to the reduction in threshold at high temperature the leakage power is also increased that increases the power consumption of a semiconductor device.

II. STEPS INVOLVED IN DTM DESIGN

For controlling the on-line temperature in electronic devices we have to follow some design procedures. They are:

- Measurement of on-chip temperature.
- Selection of proper configuration
- Estimate the device temperature.
- Compare the results with fixed maximum threshold value.
- Measured temperature exceeds the maximum threshold value perform cooling function otherwise repeat from step2.

  The following flowchart will illustrate the above steps.

2.1 Measurement of Power consumption

The total power consumption of a CMOS circuits can be expressed as

$$P_{total} = P_{dynamic} + P_{static}$$

$P_{dynamic}$=Dynamic power consumption.

P_{static}=Static power consumption.

Dynamic power consumption also includes the short circuit power. The first one occurs due to the change in the states of logic gates and second one occurs when both N-type and P-type devices are turned on.

$$P_{dynamic} = f_{c/k}.C_{eff}.\eta.V_{dd}^{2} + f_{c/k}.\eta.I_{short-circuit}.V_{dd}$$

Where, $f_{c/k}$ is the clock frequency, C_{eff} is the effective capacitance, η is the activate factor, V_{dd} is the power supply Voltage and $I_{short\text{-}circuit}$ is the average short circuit

2.2 Design of chip package

Figure.1. illustrates the normal chip package which has two heat removal paths. Thermal interface material (TIM), silicon bulk, heat spreader and heat sink are referred as primary heat removal paths. The secondary heat removals paths include interconnect layers, pads and the printed circuit board (PCB).

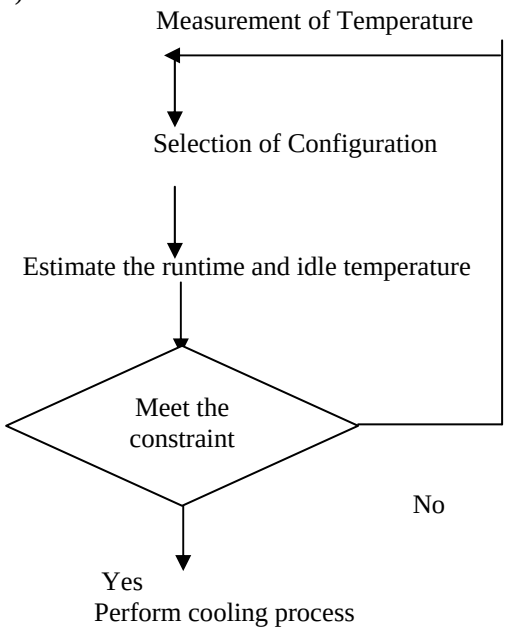
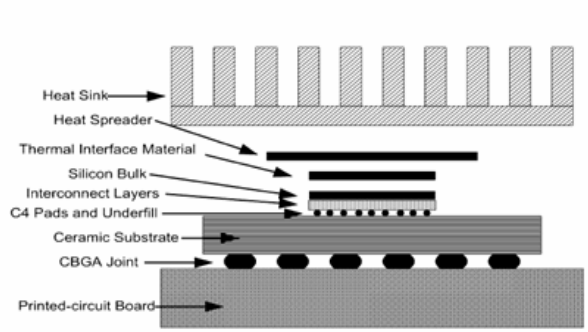


Fig.1 Cooling Process



In three-dimensional IC's the heat dissipation pass through some of the interconnected layers having extremely low thermal conductivity materials. For this IC design micro fluid channel heat removal mechanism is proposed. In which the IC is fabricated within a silicon bulk and fluid is passed through it to remove the heat.

III. HEAT MANAGEMENT APPROACHES

The temperature can be controlled by controlling the chip cooling system or the chip power consumption profile. The schemes available for cooling system are based on power-saving or noise issues. DTM methods are used to control the power consumption profile. The classifications of different approaches are given below.

3.1. Hardware Approaches

Hardware power dissipation is the source of temperature increasing. To control this we have to run the hardware under different configurations. Most adoptable configuration is through dynamic voltage/frequency scaling (DVFS). The power consumptions of the components are associated with power supply voltage level and the dynamic terms are associated with the switching frequency. .Controlling the power supply level and clock frequency, we can get different power consumptions at different levels.

3.2. Software Approaches

In multi-core processors, by using task migration the dynamic control of power profile can be achieved. Since the power consumption is input dependent, we have to assign different tasks to different functional units or processor cores. In this way the Power consumption is distributed out with some hotspot temperature constraints.

3.3 Design of Architecture

By using effective run-time architectural designs the.DTM method controls the power consumption.

IV. MEASUREMENT OF ON-CHIP TEMPERATURE

The essential part of DTM design is to measure the Temperature. For fixing guard band for temperature constraints accurate temperature measurement is essential. To avoid performance degradation, DTM should have accurate temperature measurement mechanisms. The most widely used way temperature measurement is the use of on-chip thermal sensors. To reduce the temperature measurement errors we have to use proper sensor replacement and thermal profile interpolation techniques.

4.1. On-chip thermal sensor

There are basically two-types of on-chip thermal sensors analog and digital. The analog sensors can produce the temperature dependent voltage/current by exploiting the phenomenon that some electrical parameters are sensitive to temperature variations. These parameters include PN-junction forward voltage, threshold voltage and leakage current. As shown in fig.2 the temperature pulse generated by a heater in the center will have a temperature dependent phase shift at the thermopiles. This sensor employs the dependent between

temperature and phase shift value to perform the temperature measurement.

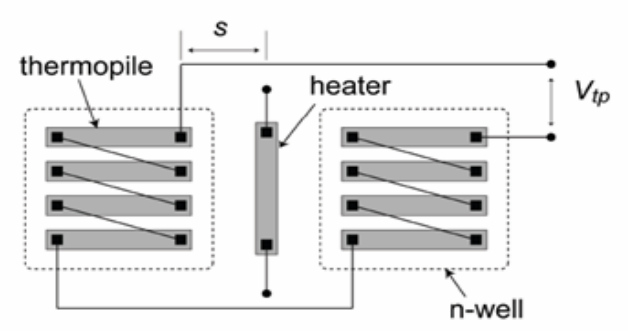


Fig.2 Thermopile heater

DTM usually requires a digital input for its control mechanism By using analog to digital converter digital thermal sensor process the given analog input signal. Among the several types of digital sensors a 4T decay sensor has been proposed. It consists of a 4T memory cell for sensing the temperature and converts it to a digital signal a decay counter.

Normally Run Oscillator (RO) is used as a on-chip thermal sensor. The high to low transition time for an inverter is:

$$t_{PHL} = \frac{2C}{\mu_n C_{ox}(W/L)_n (V_{DD} - V_t)} \left[\frac{V_t}{V_{DD} - V_t} + \frac{1}{2} l_n \left[\frac{3V_{DD} - 4V_t}{V_{DD}} \right] \right]$$

Where, μ_n & V_t are temperature dependent parameters. The RO frequency and temperature conforms a linear relationship around the point we would like to observe.

4.2. Sensor Error

It is important to place the thermal sensors in accurate locations for monitoring accuracy because they occupy chip area, consume power & increase calibration cost. The relationship between the accuracy of a temperature reading and the distance of the sensor from a hotspot is formulated as:

$$T(r) = T_{\max} \times (1 - e^{-2r/k})$$

V. EXPERIMENTAL RESULTS

Fig.3. shows the delay and leakage improvement under different delay relaxation at time 0 for C5315. The figure shows that the more delay relaxation is, the more delay and leakage improvement will be, since more replaced gate will lead to less leakage and smaller NBTI degradation. To get a tradeoff between the circuit delay at time 0 and after 10 years, we prefer the 8% delay relaxation at time 0 in our simulation and the comparison is given in Fig4.

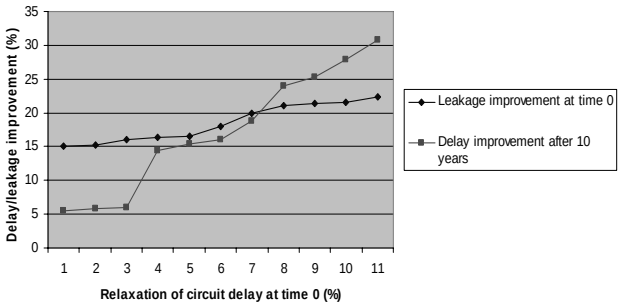


Fig.3. Leakage and NBTI improvement under different delay relaxation at time 0.

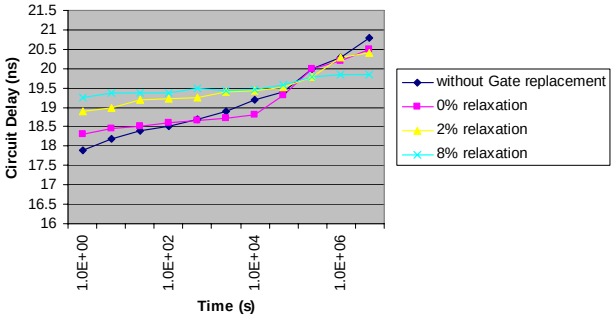


Fig.4. NBTI-induced delay after gate replacement under different delay relaxation at time 0.

Fig.5 shows the DGR results for C880 under different weighted object function [different weight ratio in the object function]. The figure shows that the value of weight ratio has large impact on the DGR algorithm results. If is small, which means the leakage has larger weight than the delay in the object function, then we get more leakage reduction but more NBTI-induced delay degradation, vice versa. So if the NBTI and the leakage are considered simultaneously, the tradeoff between the leakage power requirement and the circuit lifetime requirement should be well balanced by designers. The impact of Ratio of active time and standby time (RAS) on leakage and delay improvement by DCBGR algorithm for co optimization is shown in Fig. 6

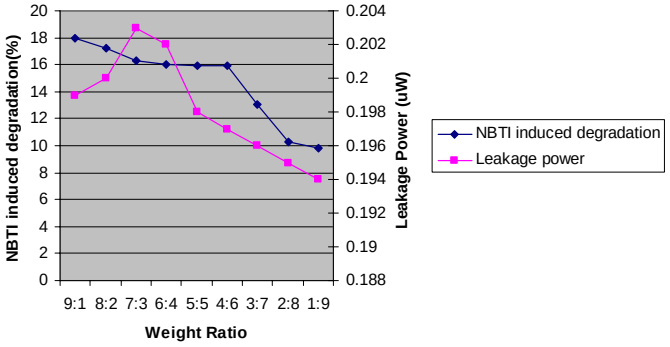


Fig.5. Leakage and NBTI-induced degradation after proposed algorithm under different weighted object function.

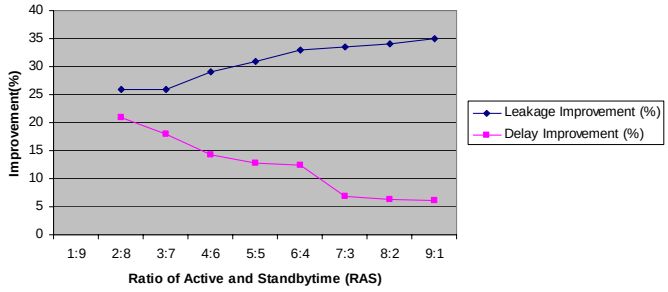


Fig.6. Leakage and delay improvement under different RAS by proposed algorithm for co optimization

Benchmark Circuits	Leakage Improvement (%)	Delay Improvement (%)	*NBTI induced Degradation*	Circuit Delay			
				without Gate replacement	0% relaxation	2% relaxation	8% relaxation
C432	29	14.2	16.3	18.4	18.52	19.2	19.36
C499	31	12.77	16.05	18.5	18.6	19.21	19.38

Table.1.Results of DTM algorithm

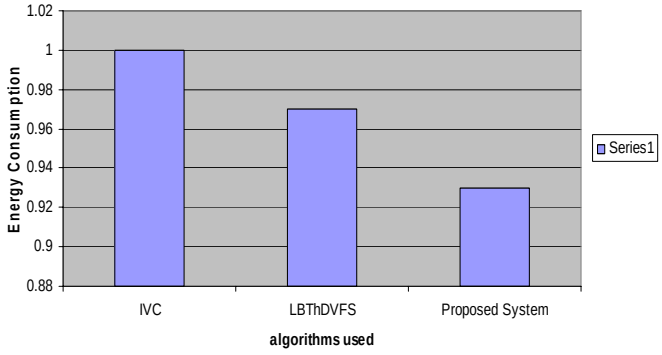


Fig.7. Comparison of Algorithms

Figure 7. Compares energy consumption of all three techniques. Our technique improves the energy consumption by 8% and 12%, respectively, in comparison to *IVC* and Load Balance with temperature-triggered DVFS *LB_ThDVFS*. The lower energy consumption is achieved mainly due to our energy aware task assignment scheme in normal mode. The energy consumption is further reduced by even distribution of heat across the chip in high utilization mode, which reduces the hot spots, biasing temperature and leakage power.

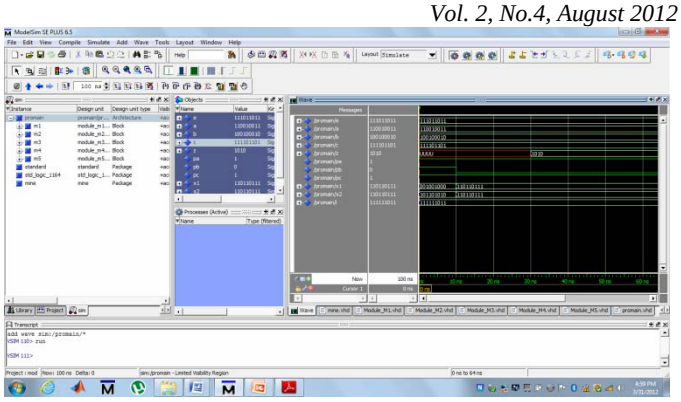


FIG.7.1 SIMULATION RESULTS OF C432

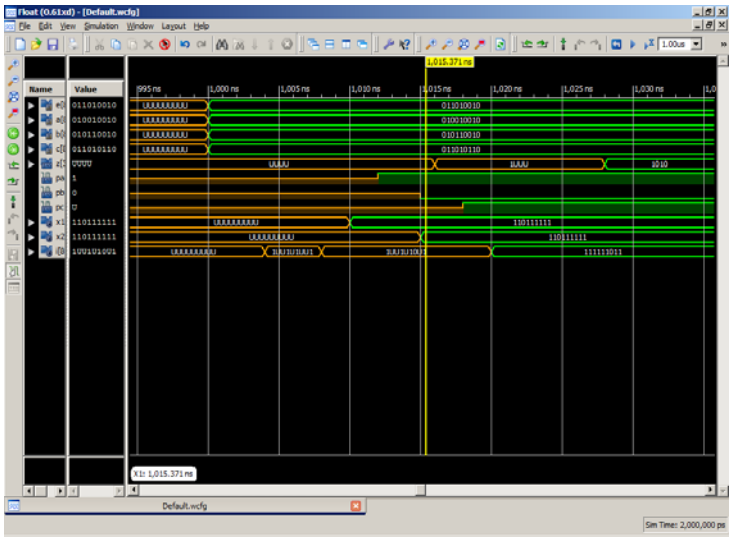


FIG.7.2 SIMULATION RESULTS OF C499 CIRCUIT 1.

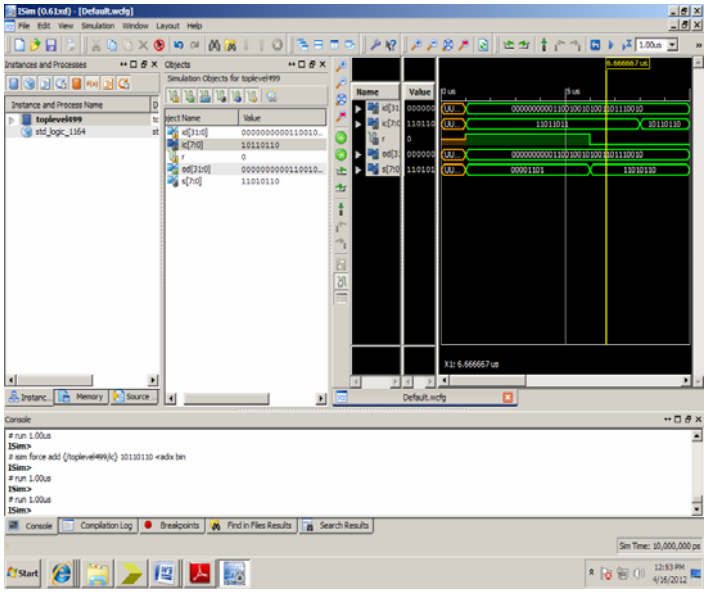


FIG.7.3 SIMULATION RESULTS OF C499 CIRCUIT 2.

CONCLUSION

As technology is scaling down we have to reduce the power consumption by reducing NBTI effect and leakage power and increase the reliability, here we propose the methodology of using DTM instead of IVC technique which only concentrate on reducing NBTI effect and it cannot be used in larger circuits. This method effectively reduce the on-chip temperature by using cooling mechanism thereby reduce the NBTI effect and leakage power.

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