Asymmetric 6T SRAM cells using a boosted bit line write assist technique

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***Abstract*—In this paper, to improve write-ability of SRAM cell a new boosted bit line voltage technique is presented. In this technique the bit line voltage is boosted up to $V_{DD}+\Delta V$. The write assist circuit consists of a CMOS which works as a boosted capacitor, $C_{P\text{-}boost}$, to produce the boosted voltage. This proposed write assist technique leads to more leakage power reduction. An asymmetric 6T-SRAM cell design is also presented for low-voltage low-power operation. This circuit is designed in 65nm CMOS technology. Increased write and read margins makes these circuits more fast and stable.**

Keywords-Boosted capacitor, SRAM, Write ability.

I. INTRODUCTION

Local random variations in device characteristics can easily lead to cell flipping during Read (Read disturb), Write failure, or Read in SRAM cells [1], [2]. Read Write failure operation and cell disturbs makes it difficult to simultaneously alleviate the various failures.

Fig. 1 shows the standard 6T-SRAM cell structure. In conventional 6T-SARM cell two back to back inverters (pull up and pull down) are connected which keep the data and its inverse on nodes Q and QB, respectively. The access transistors are used to perform read and write operations. Due to using a common path (through access transistors) for read and write operation, if we are improving the write ability then this will lead to degradation in read ability of cell and if we improve the read ability this will also lead to degradation in write ability [3]. In conventional 6T-SRAM cell write ability can be improved by dynamically altering the word-line or cell supply voltage using row or column based control [4]-[8]. A reduced cell supply voltage (weaker pull-up devices) or higher word-line voltage (stronger access transistors) during Write operation improves cell write ability [5]-[6]. To improve the Read Static Noise Margin (RSNM) of cell, beta ratio (β=WPD/WAC) can be increased. To improve the SRAM cell write ability alpha ratio (α=WPU/WAC) should be lower.

In this paper, a new asymmetric 6T-SRAM cell with boosted bit line technique is proposed which can improve read and write performance with less area. The asymmetric 6T-SRAM cell uses transmission gate as access device which improves the write ability of the cell. In addition, using a new write assist technique circuit improves the strength of the cell and it allows SRAM to work at lower supply voltages and this leads to lower leakage power consumption.

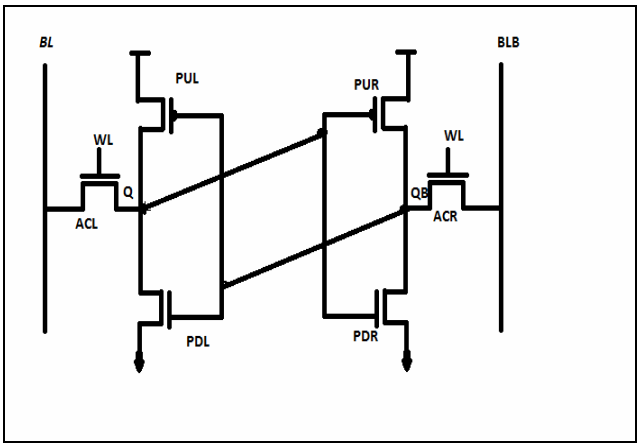

Fig.1. The standard 6T SRAM cell

The rest of the paper is arranged as follows. In Section II, a brief survey of existing asymmetric SRAM cells is presented. Section III presents the logic design and operation. Section IV includes circuit implementation of digital circuits. Simulation waveforms and power comparison table is in section V. and section VI focuses on conclusion.

II. DIFFERENT SRAM TOPOLOGIES

In this section, the asymmetric 5T SRAM cell and a write assist technique is discussed after this to improve the write ability a SRAM cell using transmission gates is discussed.

A. Asymmetric 5T SRAM cell

In this section cross coupled inverter of different sizes are used to increase the RSNM of the standard 6T SRAM cell at the cost of write margin reduction during write '1'. The asymmetric 5T-SRAM cell is shown in Fig. 2. Two different sizing scenarios: (i) maximum RSNM (RSNM Max) and (ii) maximum WM (WM Max) are used. In 5T asymmetric SRAM cell two inverters strong pull down transistor (DL) and minimum size pull down transistor (DR) are used. Minimum

size pull down transistor (DR) in the inverter with input connected to Q (right hand) increases its trip point and using the strong pull down transistor (DL) connected to the access transistors decreases the increment in the voltage of storage node (VQ) during read [3].

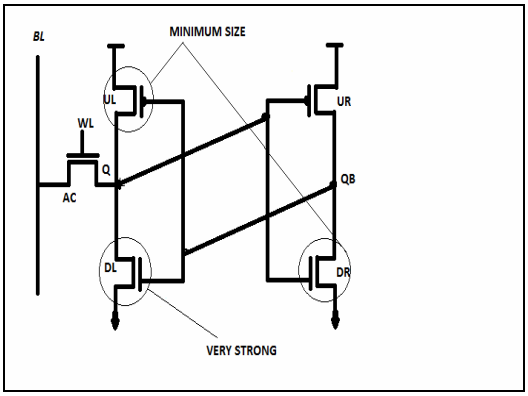

Fig.2 The asymmetric 5T SRAM cell

B. *Boosted word line and negative bit line write assist techniques*

Many write assist techniques have been proposed to improve write margin of SRAMs. The techniques are Boosted Word-Line (BWL), cell VDD collapse [14], cell GND boost and Negative Bit-Line (NBL). Amongst the existing proposed techniques, Negative Bit Line (NBL) write assist is the best technique to reduce SRAM minimum supply voltage, when considering dynamic failure metrics. NBL technique improves the write ability of '0' because NMOS ideally passes the '0' and PMOS passes '1'. The NBL technique is appropriate for the dual bit line cells. So this technique improves the write ability of '0' but it cannot be applied to the 5T-SRAM cell during write '1' operation.

In boosted word line technique, during write operation the word line voltage (V_{WL}) connected to the gate of AC transistor (Fig. 2). This boosted word line voltage increases the gate source voltage of AC (V_{GS-AC}) and improves its drivability. During write '1' operation, V_{GS-AC} will be decreased by increasing V_Q. This decreased voltage leads to significant decrease in access transistor drivability. So BWL technique is not appropriate to write '1' operation. It's a drawback of asymmetric 5T SRAM cell.

Cell VDD collapse and cell GND boost techniques in asymmetric single-ended cells are much less effective than the NBL write assist technique because these techniques degrade the Hold Static Noise Margin (HSNM) of the half- selected cells and are not suitable for low voltage applications.

C. *The asymmetric 6T SRAM cell*

The asymmetric 6T SRAM cell is shown in fig 3. Unlike the standard 6T SRAM cell back to back inverters are connected to achieve the higher RSNM. To keep the RSNM sufficient high and to solve the issue of write '1' in 5T SRAM cell one modification is done. The NMOS access device is replaced with a transmission gate. In 5T SRAM cell, suppose that the store node Q holds '0' and we wants to change to '1' during a write cycle, when the write cycle starts, the strength of the access transistor (AC) is maximized(VGS-AC=VWL). As soon as the voltage of node Q='0' starts to increase, VGS-AC starts to decrease. As a result, the strength of AC is reduced and the access transistor enters the cut off region at VQ=VWL-VTH-AC. This is the main disadvantage of 5T SRAM cell.

Replacing the NMOS access device with a trans- mission gate, one of the NMOS or PMOS transistors would always continue to conduct during the write mode with the maximum strength. In proposed 6T SRAM cell paths for read and write '1' is separated from each other. In the proposed asymmetric 6T-SRAM cell, the bit-line is pre charged to GND and then the transmission gate access device is enabled. If Q='1', the BL will be charged to VDD through the cell (instead of discharging) during the read cycle. By using this method, a minimum size pull-down transistor can be used which helps writing '1'.

During read operation, the BL is discharged to ground and the PMOS access device turns on while NMOS is kept OFF to achieve a higher RSNM. In case when node Q stores '1', the BL will be charged through transistors AP and UL. Hence, RSNM improvement can be achieved by the use of a stronger pull-up transistor (UL) that will help writing '1'.This means that, in the proposed cell, RSNM and write margin can be simultaneously improved.

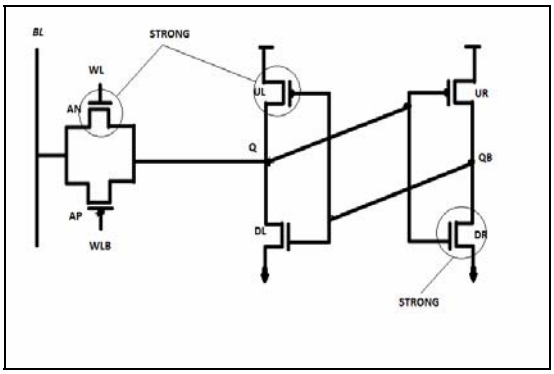

Fig.3 The asymmetric 6T SRAM cell using TG

D. *Boosted bit line write assist technique*

The boosting bit line approach is found to be the best write assist technique. Fig. 4 shows the asymmetric 6T-SRAM array and the implementation of the write assist circuit. In the write assist circuit the bit line voltage is boosted up to VDD+ΔV. The minimum ΔV voltage has to be chosen in such a way that sufficient write '1' improvement is achieved if ΔV will be high then it leads to an increase in the leakage current of the cell. Boosted bit line technique gives the better write margin but at the cost of high power dissipation, delay and large area. To overcome these drawbacks some modification is done in the boosted write assist circuit.

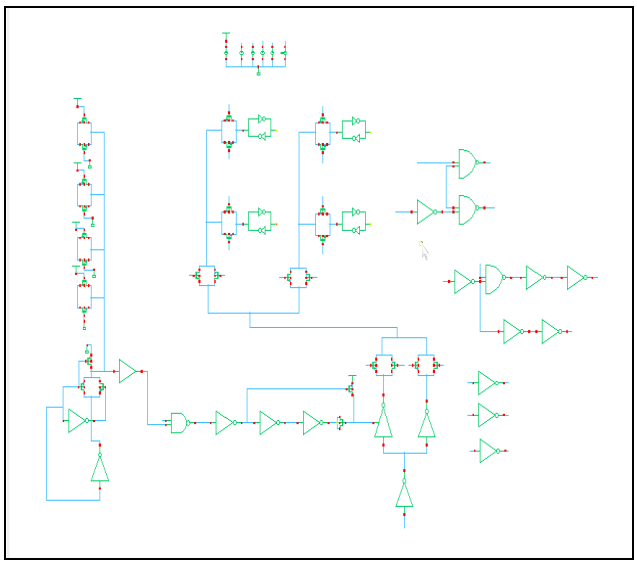

Fig.4 Schematic of write assist Circuit.

III. PROPOSE ASYMMETRIC WRITE ASSIST CIRCUIT

In this section improved write assist circuit is proposed which removes the drawback of previous write assist circuit. In the proposed write assist circuit boosting capacitor is replaced by a CMOS circuit. Data and Data bar control signals are used in place of C1 and C2.Data is directly inserted at the data node. So some of the extra gates are removed which leads to decrease in area and less power dissipation.

The replica column consists of 2n turned off transmission gate cells plus the replica column driver for an n × m array. In this circuit CMOS used as a capacitor to produce the boosting voltage. The replica column is used to determine the best time for connecting the CMOS (as a boosting capacitor) to BL. When the replica column bit line (RBL) charges to VDD/2, BL is charged to VDD. The absolute value of the gate-source voltage (Vgs) of the PMOS transistor of the transmission gate of the selected cell connected to BL (AP) will be increased. This improves the write ability of the cell while writing '1' and makes the PMOS access device stronger.

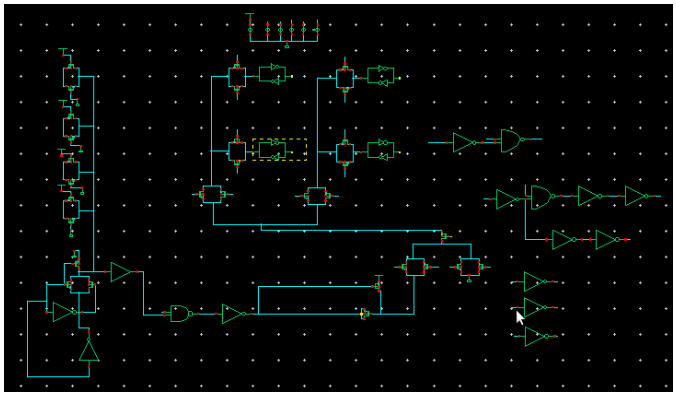

Fig.5Schematic of proposed write assist Circuit.

IV. CIRCUIT IMPLEMENTATION

A. *Design and implementation of 6T SRAM cell*

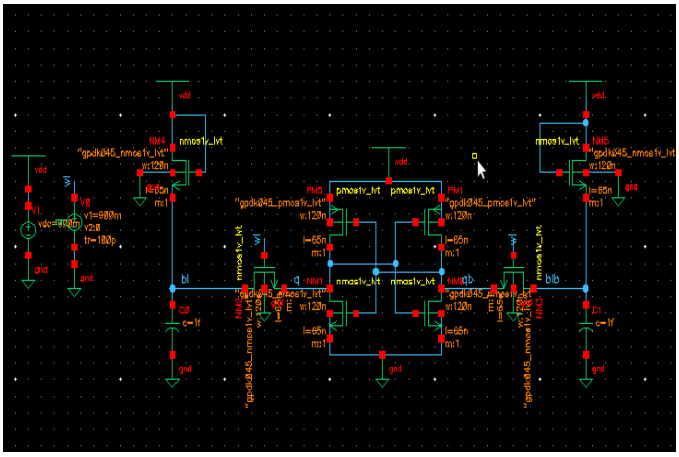

Fig.5 Schematic of 6T SRAM cell

B. *Design and implementation of asymmetric 5T SRAM cell*

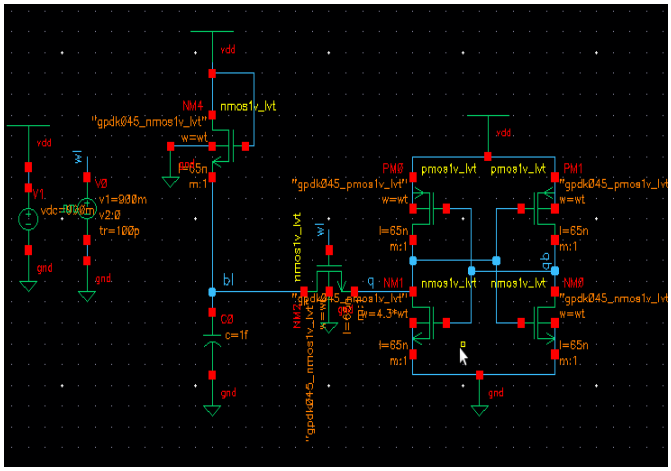

Fig.6 Schematic of 5T SRAM cell

C. *Design and implementation of 6T SRAM cell using transmission gates*

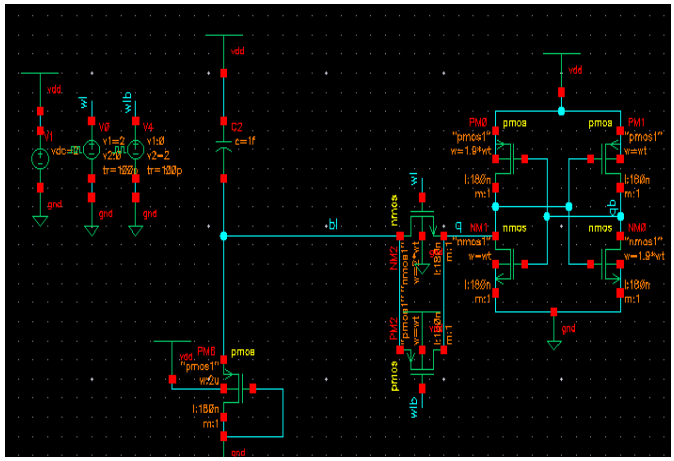

Fig.7 Schematic of 6T SRAM cell using TG

V. SIMULATION RESULTS AND WAVEFORMS

A. Butterfly curves for 5T (WM max)SRAM cell

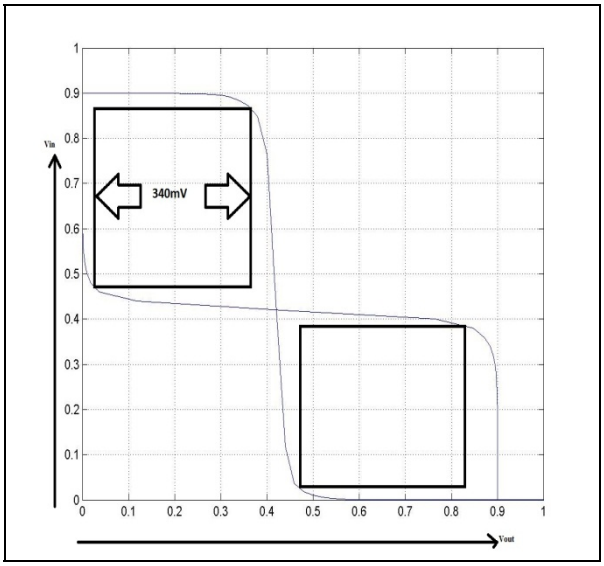

Fig.8 Butterfly curve for 5T (WM max)

B. Butterfly curves for 5T(RSNM max)SRAM cell

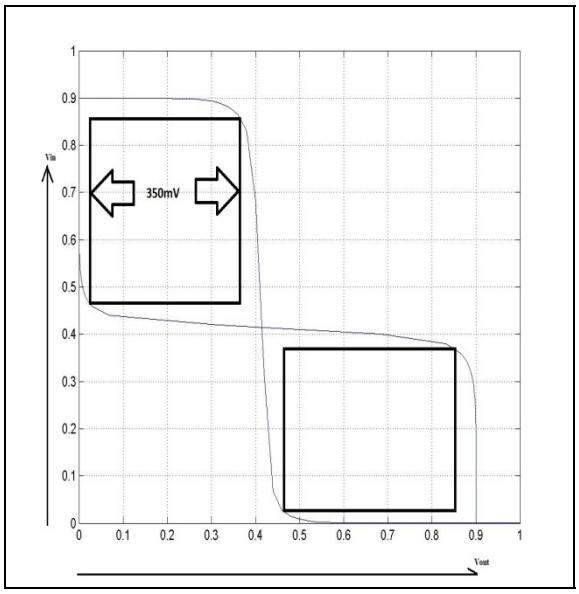

Fig.9 Butterfly curve for 5T (RSNM max)

C. Butterfly curves for standard 6T SRAM cell

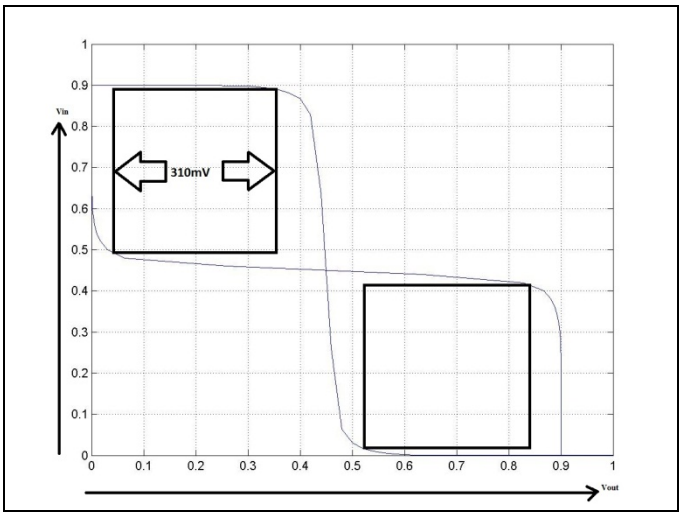

Fig.10 Butterfly curve for 6T SRAM cell

D. Butterfly curves for 6T SRAM cell using transmission gates

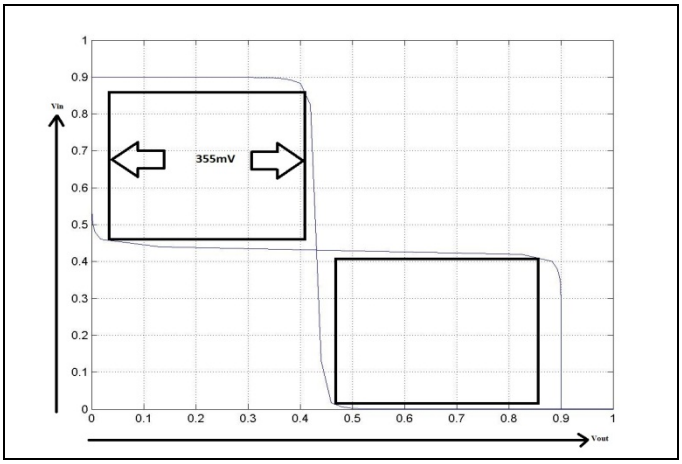

Fig.11 Butterfly curve for 6T SRAM cell using TG

E. The layout of standard 5t (wm max)

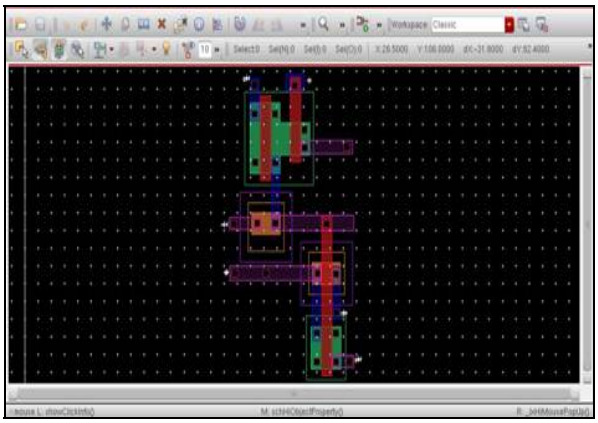

Fig.12 Layout of standard 5T (WM max)

F. The Layout Of Standard 6T

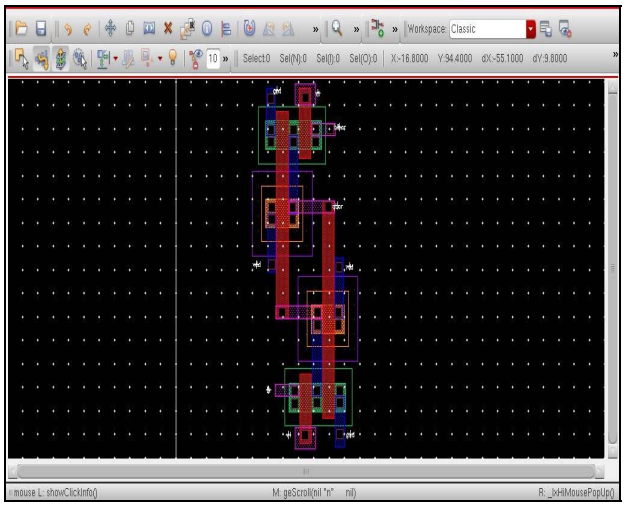

Fig.13 Layout of standard 6T

G. The Layout Of 6T using Tgs

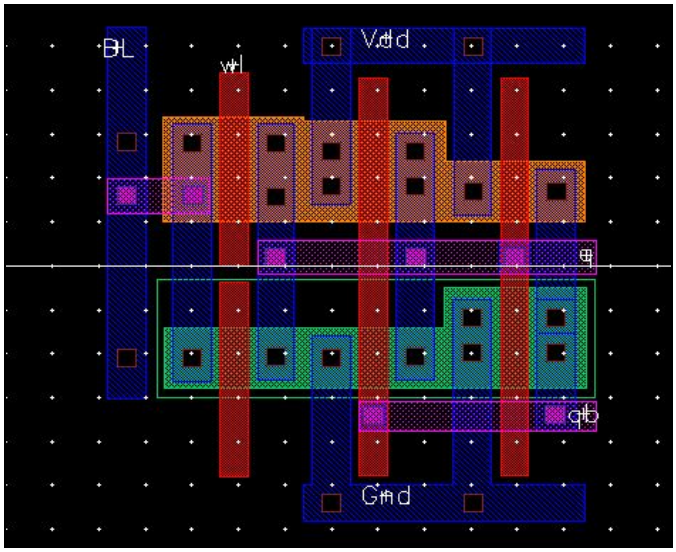

Fig.14 LAYOUT OF 6T USING TGS

TABLE I. LEAKAGE CURRENT Q=0

6T Symmetric	6T Using Tgs	5T for max RSNM	5T for max WM
Across n2= 1.195p	Across tg= 6.321p	Across n2= 45.2u	Across n2= 55.413u
Across p5= 23.41p	Across n0=14.1427p	Across n0= 361.4p	Across n0= 2.47n
Across n0= 41.39p	Across p0= 2.40p	Across p0= 22.5p	Across p0= 65.05p
Across n3= 41.39p			

TABLE II. LEAKAGE CURRENT Q=1

6T Symmetric	6T Using Tgs	5T for max RSNM	5T for max WM
Across n2= 1.3964p	Across tg= 9.09n	Across n2= 517.215p	Across n2= 682.324p
Across p1= 23.419p	Across n1= 21.1663n	Across n1= 82.78p	Across n1= 72.2215p
Across n1= 41.39p	Across p1= 7.70n	Across p1=23.4091p	Across p1=23.4081p
Across n3= 310.19p			

TABLE III. WRITE ASSIST TECHNIQUE PARAMETERS

Parameters	Boosted bit line	Modified
Power	4.91u	2.12u
Delay	10.47n	862.25p

TABLE IV. AREA OF LAYOUT CELL

Standard 6T	6T using Tgs	5T for max RSMN	5T for max WM
2.55 um^2	2.49 um^2	2.95 um^2	2.76 um^2

TABLE V. CALCULATEDRSNM

SRAM Cells	Values
5T RSNM	350 mV
5T WM	340 mV
Standard 6T	310 mV
6T using TG	355 mV

TABLE VI. CALCULATEDWM

SRAM Cells	Values
5T RSNM	0.9-0.8069 = 0.0931 mV
5T WM	0.9-0.7192 = 0.1808 mV
Standard 6T	0.9-0.7002 = 0.1998 mV
6T using TG	0.9-0.6831 = 0.2169 mV

VI. CONCLUSION

In this paper a write assist technique is used to enhance the write ability of the SRAM cell using transmission gates and further modification is done in the write assist circuit to reduce the power consumption and delay. The proposed circuit gives the better results. The result shows that the SRAM cell with transmission gates achieves higher RSNM as compare to the standard 6T and 5T SRAM cell.Write margin of the 6T SRAM cell using tgs is around 50% higher than the standard 6T SRAM cell. In proposed write assist circuit the leakage power decrease up to more than 60%, less area and less delay is achieved. Simulation results also shows that the leakage is more in 5T and standard 6T cell as compare to the 6T SRAM cell using transmission gates.

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